ALMA Test Interferometer Project Book, Chapter 8

IF Processing and Data Transmission

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Summary

This Chapter describes the signal processing from the IF outputs of the front end through the baseband digital inputs of the correlator. Accordingly, it includes

1) the intermediate frequency (IF) down-converter
2) the digitizers
2) the fiber optic digital link

The signals from the active receiver at each antenna will pass through an IF selector switch and into an IF down-converter. The down-converter analog output signals will then go to digitizers, then to the fiber optic link which will carry the signals to the central electronics building, then into the correlator.

8.1 IF Down-Converter

The IF down-converter for the Test Interferometer uses the same design, with a few minor variations, as that proposed for the ALMA telescope. In this way the design can be developed and thoroughly tested before going into quantity production for ALMA.

In the Test Interferometer, the two inputs to the single down-converter module will be the two polarization signals from the front-end. In the ALMA telescope, there will be two down-converter modules at each antenna, one for each polarization, and the two inputs to each module will carry upper and lower side-band signals.

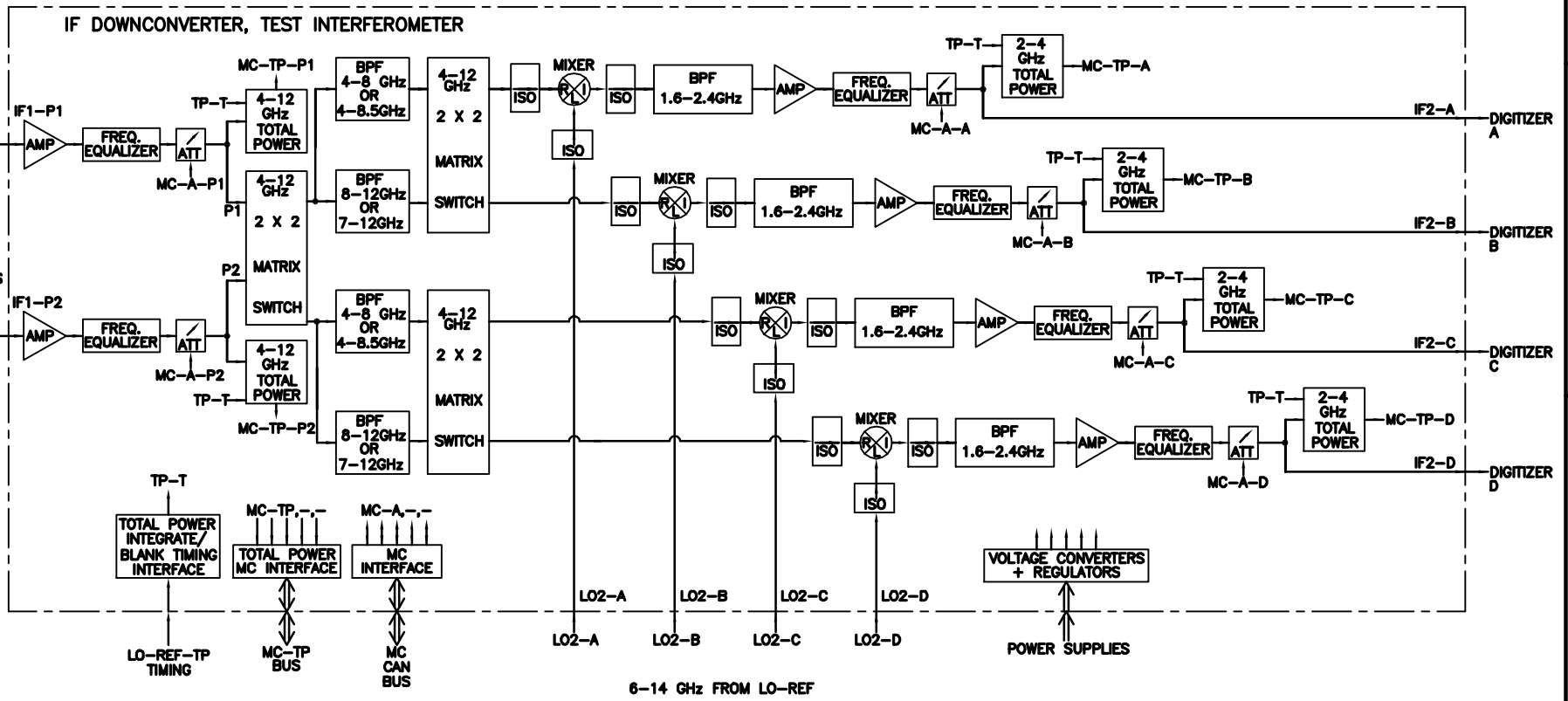
A block diagram of the down-converter in its Test Interferometer variation is shown in Figure 8.1 and the specifications are in Table 8.1. The input and output nosie spectral power distribution will be nominally flat over the band-pass as given in the specifications.

The down-converter will take the wideband 4 - 12 GHz input signals received from the front-end system and produce four output signals each with a band-pass of 1.6 to 2.4 GHz suitable for band-pass sampling at the digitizers, which in the Test Interferometer are clocked at 1.6 GS/sec.

In addition to gain, frequency conversion and band-pass definition, the down-converter module provides total power measurement of both the two wideband input signals and the four narrowband output signals, plus a switching capability which allows any output channel to tune either the upper or lower frequency portion of either input channel (4-8 GHz or 8-12 GHz).

In discussing the specifications for the down-converter, the following definitions are used; values within square brackets [ ] are tentative. Values To-Be-Determined are marked TBD.

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



ACAD : TI–IFDC–CBD

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES : ANGLES ±	1°
3 PLACE DECIMALS (.000) ±	.0005
2 PLACE DECIMALS (.00) ±	.005
1 PLACE DECIMALS (.0) ±	.01
	.1

MATERIAL :

FINISH :

ALMA PROJECT : ALMA–US–D&D TEST–INTERFEROMETER IF DOWNCONVERTER

TITLE : CONCEPTUAL BLOCK DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	M. SULLIVAN	DATE 2/9/00
DESIGNED BY	B.BRUNDAGE	DATE 2/8/00
APPROVED BY		DATE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER TI–IFDC–CBD | REV. – | SCALE NONE

Define *signal-to-noise-ratio (SNRx)* at IF system location x as the ratio of total system noise spectral power to the equivalent internal noise spectral power looking downstream. SNRx will be > [30] dB at all IF locations.

All frequency conversions will have *image suppression (I) > [30] dB* throughout the passband. Mixer image noise will be included in all designs.

Define IF *headroom (Hx)* at IF system location x as the ratio of available *third order-intercept power (IP3)* to the *normal total system noise power (Pn) - 20 dB* at location x. Typically, detrimental non-linear effects of gain compression and inter-modulation occur when the IF total power exceeds IP3 - [20] dB. For example, if H = 0 dB, then the power of the 3rd order intermodulation frequency will be 2x20dB = 40 dB below the lower powered of the two intermodulating frequencies. Hx will be > [10] dB at all IF locations.

Define IF *Group Delay Variation (Δ GD/Δ t)* as a time delay per unit frequency interval per unit of time in units of nanosec/GHz/60minutes from system input to system output. Table 9.2 specifies Δ *GD/Δ t from IF inputs to outputs* as < [TBD] nanosec/GHz/[60] minutes. If D&D implements analog IF transmission over fiber, then the FO transmission is embedded in this specification. Note GD in terms of a measurement of phase vs frequency (via a vector network analyzer) is GD = $\Delta \Phi / (\Delta f * 360^\circ)$.

Table 8.1 IF Down-Converter Module Specifications, Test Interferometer

Number of modules	
Test Interferometer	one per antenna
ALMA	two per antenna
IF Input	
Number of IF inputs per module	two
Frequency	4 -12 GHz
Power level	[-30 dBm]
Headroom	>20 dB
LO Input	
LO inputs per module	four, independently tunable
Frequency	6 - 14 GHz
Power level	[+10 dBm]
IF Output	
Number of IF inputs per module	four
Frequency	1.6 - 2.4 GHz
Power level	TBD
Headroom	TBD
Conversion stability, input to output	
Gain stability in time	<2 dB p-p, 2 GHz bandwidth over 60 minutes
Band-pass ripple	TBD dB p-p, over 2 GHz, in [2 MHz] segments
Band-pass stability	TBD dB p-p, over 2 GHz in, [2 MHz segments], 60 min
Total Power Detectors	
Number on input	two, one for each input channel
Number on output	four, one for each output channel
Linearity	< 1% deviation, -3dB to +7 dB relative to nominal
Resolution	TBD
Stability	TBD in TBD seconds
Interface	Special total ower bus to antenna M/C system
Readout	Sigma/Delta A/D converter to M/C interface
Attenuators	
Input	[0.5] dB steps, range TBD
Output	[0.5] dB steps, range TBD

8.2 Digitizers

<to be written>

8.3 Fiber Optic Digital Link, Test Interferometer

The current plan for the serialization, synchronization and transmission of the digital data from the ALMA test interferometer antennas to the correlator is presented here. The fiber optic link for the test interferometer uses the same design as that intended for ALMA, with the addition of rate converter modules at the input and output which interface the 125 MHz fundamental clock rate of the link to the 100 MHz clock rate of the test interferometer digitizers and correlator.

A complete description of the link will be given in an ALMA memo "Digital Transmission of the IF Data for the Atacama Large Millimeter Array", by Edmans and Jackson to be released in the second quarter of 2000.

The link, starting from the antenna, consists of a rate converter, a digital multiplexer, an optical modulator and transmitter, a wavelength division multiplexer/ de-multiplexer, an optical receiver, and finally a digital de-multiplexer.

The basic link takes as input 32 2-bit signals from the two samplers of the test interferometer at a 100 MHz clock rate. These are re-clocked to 32 2-bit signals at 125 Mb/s and multiplexed x5 up to 625 Mb/s in a Xilinx FPGA and multiplexed again to 10 Gb/s. This output channel has 2 Gb/s spare capacity to allow for synchronization signals and 8b/10b coding. The reverse process occurs at the receiving end, outputting 32 2-bit signals at 100 MHz to the correlator.

One such link will be sufficient for the test interferometer. Eight or twelve links will be needed for ALMA depending on whether 2 or 3-bit signals are transmitted from the antenna. This full system will be largely a matter of replicating the prototype system. A full twelve link system is shown in Figure 8.2.

8.3.1 Transmitter

A block diagram of the Digital Fiber Optic Transmitter is shown in Figure 8.3. This diagram shows the data transmission system for a single channel for simplicity.

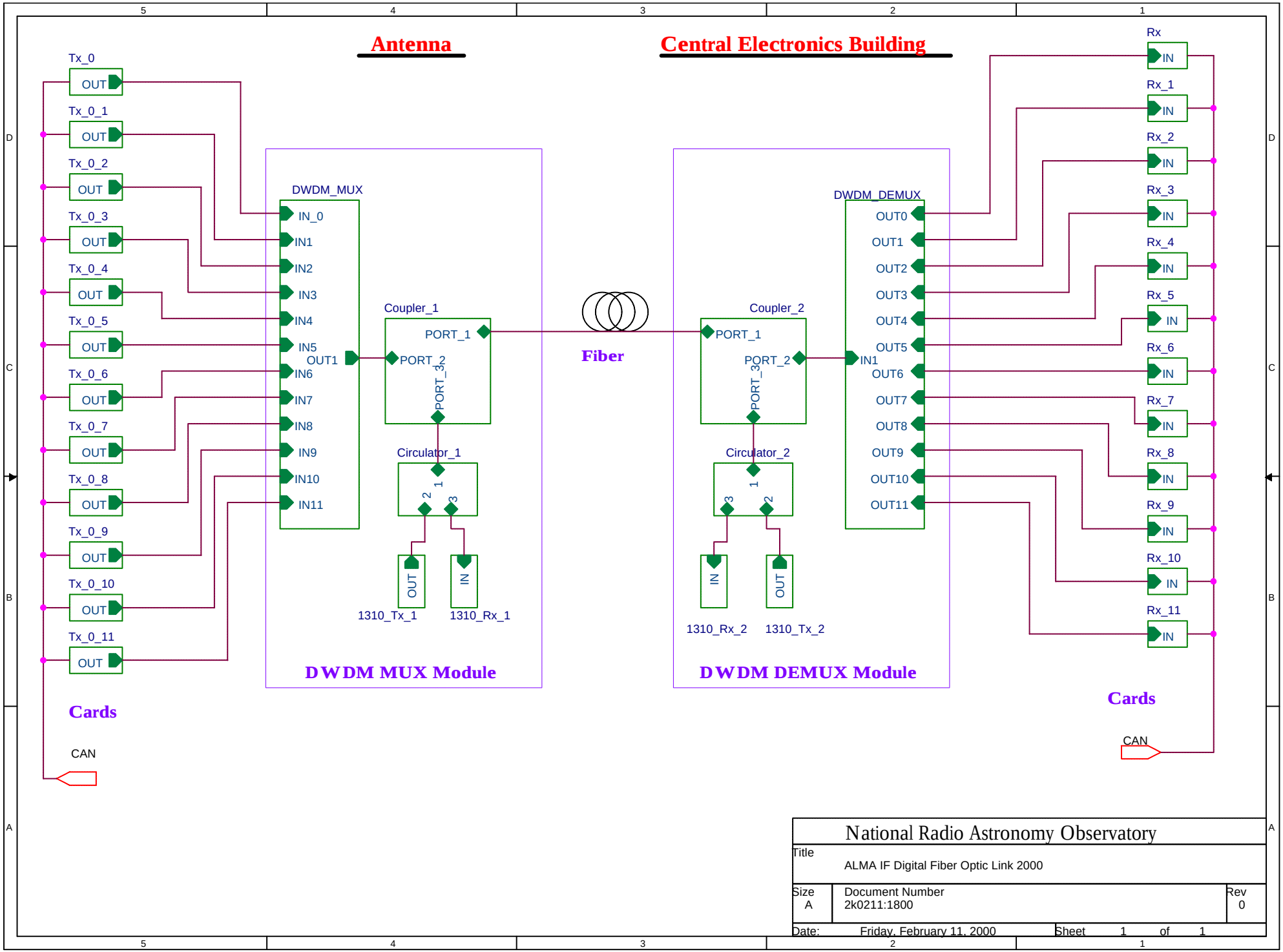
The current design contains all of the multiplexing and electrical to optical conversion on a single Euro-card style board with connections to the digitizers on the backplane. The optical to electrical conversion hardware includes the laser, laser temperature and bias current control hardware, optical modulator. In addition, there is a provision for an optical wavelength locker and the required feedback control circuit. Optical power monitoring is handled through the interface to the Laser Driver module. The card is controlled by a Monitor and Control (M&C) interface. The following list specifies the components in each element of the digital block.

M&C interface: This includes an Intel 82527 CAN controller and PIC 16C74 microcontroller. A relatively straightforward micro-controller design provides all necessary control signals and an interface to the rest of the system. The microprocessor controls the laser power and laser temperature control modules.

Clock distribution: This block includes the generation of a 625 MHz clock from the 125MHz system clock, and a 312.5 MHz clock for the FPGA. The 625 MHz clock is used for the Multiplexer.

Sync Controller and Data Routing: A Xilinx Virtex-E FPGA is included in the design. This device will contain all of the logic for routing the 125 MHz input data to the appropriate shift registers. Any 8B/10B coding or PRBS generators and/or sync pattern generators required in the design can be implemented in the FPGA.

LVDS to CML/ECL conversion: This block contains the LVDS to CML/ECL conversion necessary



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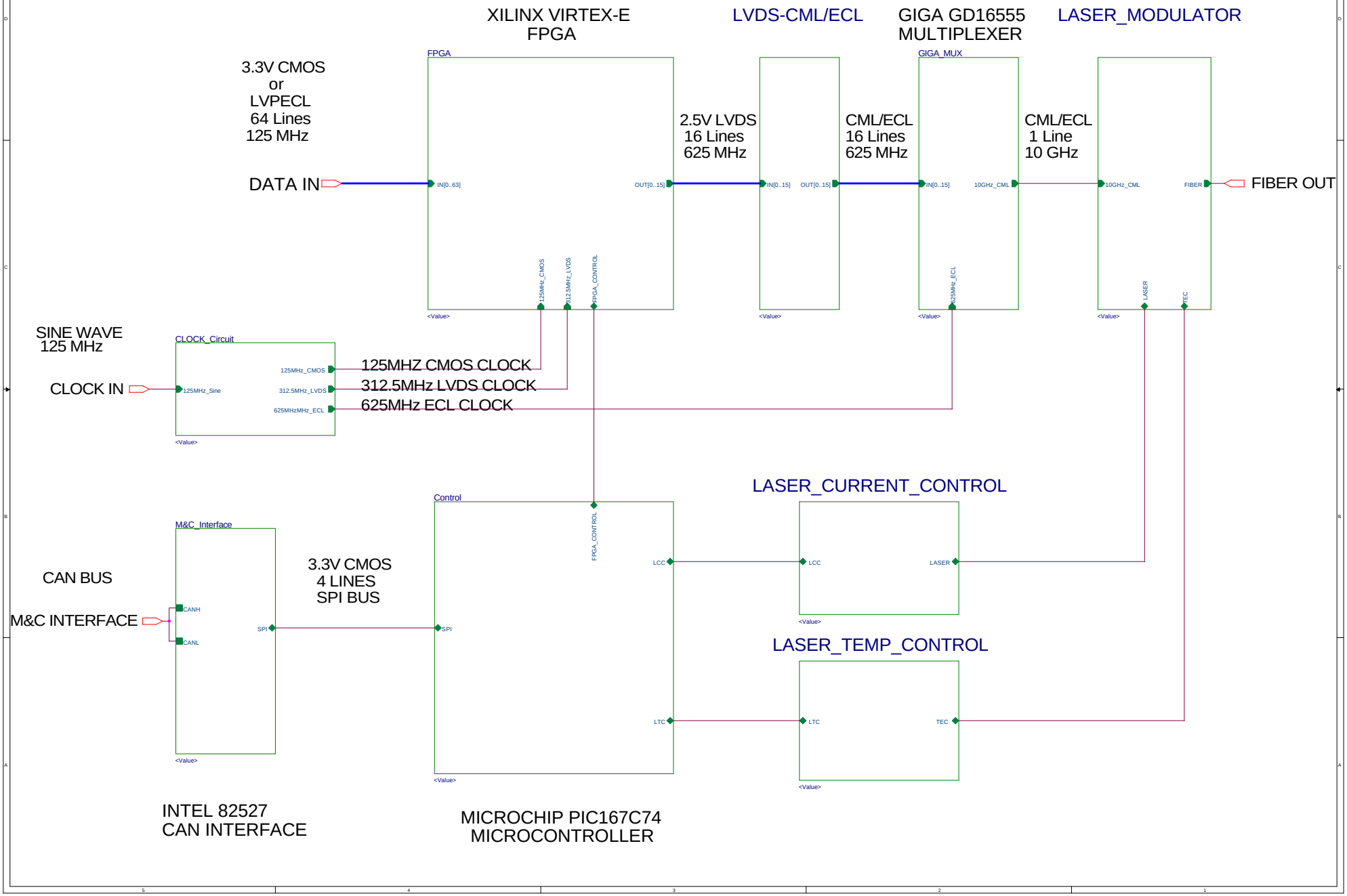
Date: Friday, February 11, 2000	Sheet 1 of 1	

FIBER OPTIC TRANSMITTER



between the Xilinx gate array and the Giga Multiplexer.

10 Gbps Serializer: This block consists of a Giga GD16555 10Gbps multiplexer IC and associated electronics. The multiplexer converts the 625MHz 16-bit parallel data into a 10 Gbps serial data stream for transmission over the fiber optic link. This circuit is essentially as shown in the data sheets, application notes and evaluation board design from Giga.

Laser & Modulator: This block includes the amplifier that is the driver for the Electro-Absorption modulator (EAM) plus the integrated laser/EAM package.

For ALMA, the output of this block is one of the 8 (or 12) WDM channels that are multiplexed together onto a single fiber in a separate optical module.

8.3.2 Receiver:

Figure 8.4 shows the block diagram of a receiver. The receiver consists of several major elements that are described here.

PD & Amps: This block contains a *p-i-n* photodiode, amplification, and an electrical filter. The output is a 10 Gbps data stream that is fed to the Giga Demultiplexer.

10 Gbps demultiplexer : The first demultiplexer stage is a Giga GD16544 10Gbps demultiplexer IC and the associated electronics. It converts the 10 Gbps serial data stream from the fiber optic link to 625 MHz 16-bit parallel data. This circuit is essentially the same as is shown in the data sheets, application notes and evaluation board design provided by Giga.

CML to LVDS Conversion: This block contains the CML/ECL to LVDS conversion necessary between the Giga Demultiplexer and the Xilinx gate array.

625MHz De-serializer: The Xilinx FPGA converts the 16 bit 625 MHz data from the Giga demultiplexer into 80 bit 125 MHz data for presentation to the Correlator. The FPGA also contains the synchronization recognition function and any decoding functions.

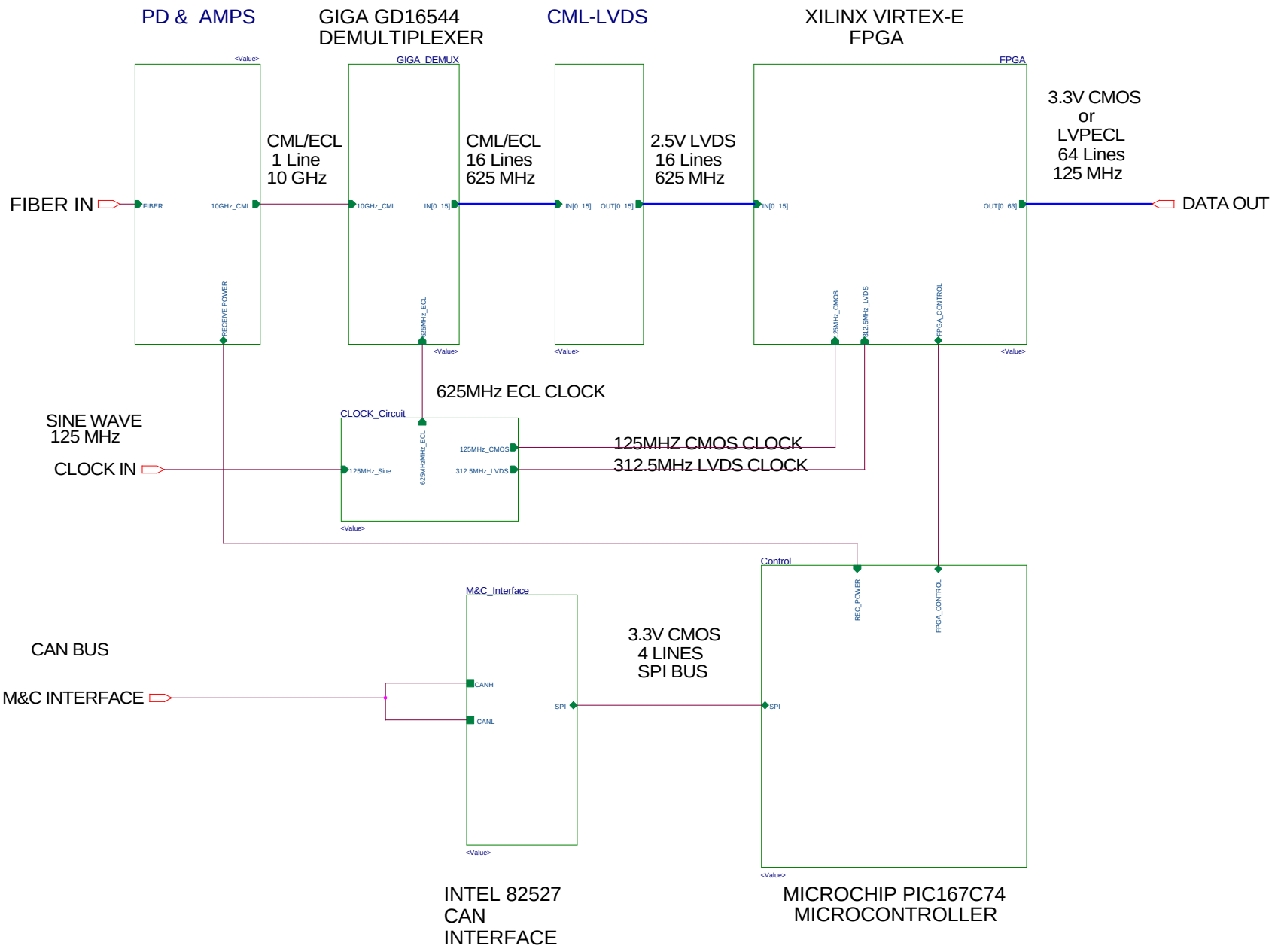
Sync Controlling and Data Routing: A Xilinx Virtex-E FPGA contains all of the 125MHz logic for routing the 125MHz input data from the appropriate shift registers to the output of the board, and any PRBS generators and sync pattern comparators required in the design. A synchronization clock control is also be implemented in the FPGA.

M&C Interface: This block contains the Intel 82527 CAN controller and a PIC 16C74 microcontroller. It is a straightforward microcontroller design providing all necessary control signals and an interface to the rest of the system.

8.2.3 Data Encoding:

In the absence of any interface specification documentation regarding the output of the ALMA digitizer or FIR filter, an optional system has been envisioned to take the place of a previously proposed 8B/10B encoding scheme. The intention is to minimize the effect of any DC offsets in the data over long run times. Dramatic DC offsets may occur, in the worst case for instance, due to hardware failures. We are using a Non-Return-to-Zero (NRZ) data format, and AC coupled amplifier stages, therefore it is possible that the data from the digitizer and FIR filter may charge the coupling capacitors between amplifier stages in the receiver. Such a situation can occur when long runs of optical logic 1's are transmitted. To ensure that the data or hardware failures do not have a detrimental effect on the performance of the fiber-optic link, two fallback schemes have been devised for implementation if necessary. Both are easily implemented in the FPGA. One scheme uses a Psuedo-Random Binary Sequence (PRBS) stream with an XOR function operating on the data so that any long runs of 1’s can be mitigated. This method can be implemented in the existing FPGA targeted for the prototype. The other alternative under consideration is simply to invert alternating words, a process that can also easily be

FIBER OPTIC RECEIVER



implemented in the FPGA. Other options exist and can also be explored.

8.3.4 Synchronization Sequence:

To synchronize the system, a predetermined bit pattern will be generated by the FPGA in the Transmitter and sent over fiber to the receiver which will search for the pattern on start-up or on demand as initiated over the M&C system. This has to be done in two stages, once to account for the synchronization of the multiplexer and a second to account for the synchronization of the serializer. The transmitter can repeatedly switch between the two patterns at some predetermined time interval. Once the receiver recognizes and syncs on the two synchronization patterns, it will signal the transmitter, via the M&C system or a dedicated low speed fiber-optic link, to send data. One variable that is as yet undetermined and which will effect the implementation is the latency in the M&C system. The total latency is the sum of the latency in the Tx and Rx cards, transmission in the optical fibers, the two CAN-bus links, the central computer, and the ATM system used to send data to the antennas. It is anticipated that this latency will be no more than one second. The following steps are required for synchronizing the system.

Synchronize the GD16555 multiplexer and GD16544 demultiplexer: - Inject a known test pattern into D0-D15 of the GD16555 multiplexer IC. In the receiver, test outputs D01-D15 of the GD16544 demultiplexer IC and determine data offset between the multiplexer and demultiplexer. This offset is stored and used to determine data routing in the 125 MHz FPGA.

Synchronize 625MHz shift registers: - Inject a known test pattern into sixteen 5-bit shift registers implemented in the transmitter FPGA. The receiver monitors the outputs of 625 MHz shift registers and switches the 125 MHz output clock through the five possible phases to determine the correct alignment. The output clock is then set to the correct phase. The receiver signals the System computer and the transmitter that it is in sync.

Once sync is recognized at both levels, the receiver signals the computer control system and the transmitter that it is in sync, and that scientific data can be transmitted.

Sync monitoring and resynchronization: – The current design has 16 unused bits in the 80 bit 125 MHz inputs. One method for monitoring synchronization is to have the transmitter continuously place a prescribed sequence such as PRBS (psuedo-random binary sequence) on one of the unused bits. The receiver would generate the same PRBS and compare the results to determine if the system is in sync. It should be possible to use this sequence to quickly resynchronize the system on the fly if synchronization is lost by only +/- a few clocks. Gross synchronization loss would require repetition of the main synchronization (steps 1 & 2). If this situation occurs, the receiver signals the transmitter to begin synchronization via the M&C system, which also flags the system.

Synchronization handshaking:
The microprocessors in each receiver-transmitter pair handshake via the dedicated link.. It has the advantage that resynchronization will take place almost instantly. This is a better alternative then handshaking through the M&C link because of the latency of communication through the M&C link which would result in a significantly larger amount of data loss should resynchronization be required.