ALMA Test Interferometer Project Book, Chapter 9

ALMA TEST CORRELATOR

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Revision History:

Summary

This section describes the ALMA test correlator. The design described here is for a lag correlator with a system clock rate of 100 MHz. This correlator is based on the design of the GBT and Tucson autocorrelator spectrometers, with provision for cross-correlation operation so that both single antenna spectra and two-antenna cross-spectra can be measured.

Table 9.1 Correlator Specifications

Item	Specification
Number of antennas	2
Number of baseband inputs per antenna	2
Maximum sampling rate per baseband input	1.6 GHz
Sampling and correlation format	2 bit, 3 level
Maximum baseline delay range	10 microsec @ 800 MHz BW
Hardware cross-correlators per baseline	65536
Product pairs possible for polarization	RR, RL, LR, LL (for circular, *e.g.*)

This correlator is intended entirely for testing the performance of the two prototype antennas, using a short baseline. The maximum delay range accommodated is 10 microsec with 800 MHz bandwidth and 80 microsec with 100 MHz bandwidth. The delay resolution is 8 samples at 800 MHz bandwidth and 4 samples at 100 MHz bandwidth. This is adequate resolution if the correlator is dumped sufficiently rapidly.
Table 9.2 below shows the principal milestones for the test correlator.

Table 9.2 Principal milestones for ALMA test correlator work

Complete hardware and internal software testing	2000-03-31
Deliver to VLA site	2000-07-01

9.1 System Block Diagram

A simplified block diagram for the ALMA test correlator is given in Figure 9.1. This diagram presents a fairly conventional lag correlator except for the presence of the data format conversion stage.

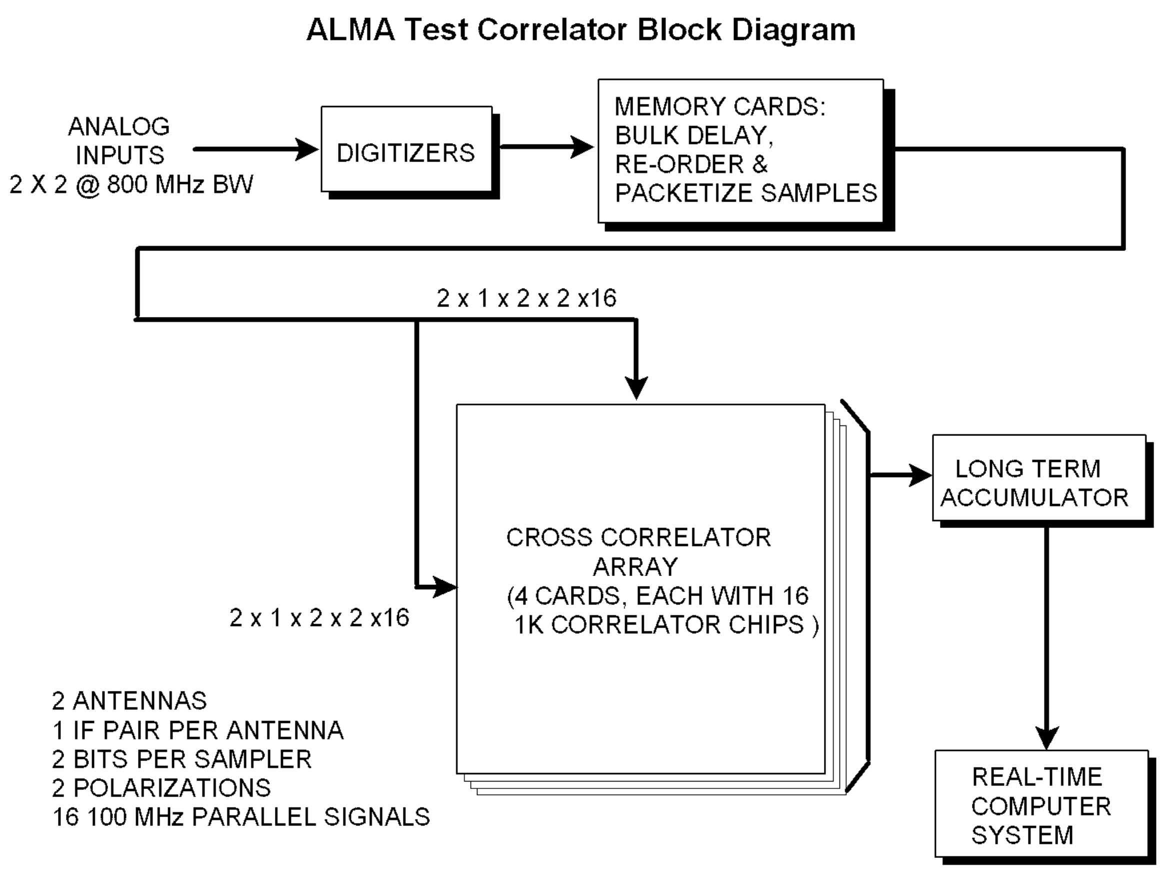

Figure 9.1: simplified correlator block diagram

The analog outputs of the baseband system, 1 polarization pair per antenna, drive four sampler inputs where 2-bit, 3-level sampling is performed at 1.6 GS/second. The analog bandwidths supported are 800 MHz and 100 MHz; bandwidths of 400, 200, and 50 MHz could be supported if a need arises.

The data format conversion block takes the 16 parallel outputs of each sampler and, using RAMs, both adjusts delays and re-sorts the samples. In this block, the 16 parallel outputs of a high speed sampler are converted from each carrying every 16th sample to each carrying short (1.3 msec) bursts of contiguous samples.

By using the format conversion scheme, the 16-wide parallel output from a sampler are transformed into 16 parallel signals, each carrying 1.3 millisecond packets of contiguous samples. This simplification in the correlator circuit requirements is obtained at the cost of an inefficiency of about 0.8% which results because the end bits in adjacent 1.3 msec time segments of samples will not get correlated.

An additional benefit of the format conversion strategy is that it allows the system the same advantage as a recirculating correlator: when the bandwidth being processed is reduced by a factor of 2, the number of lags the system is capable of generating goes up by a factor of 2. This results in a factor of 4 increase in frequency resolution for a factor of 2 decrease in bandwidth.

The custom lag correlator chip provides 1K lags and is the "Quaint" chip designed by John Canaris. The chip can be programmed via a microprocessor supplied program word.

The long term accumulation block seen in figure 9.1 integrates the correlator outputs for the desired duration.

9.2 Performance

This section gives performance parameters for the operating modes of the ALMA test correlator.

Table 10.3 below gives the supported autocorrelation modes.

Table 9.3 Autocorrelator modes

Bandwidth (MHz)	Number of antennas	Number of IFs per antenna	Number of spectral channels	Frequency resolution (kHz)
800	2	2	1024	781
100	1	2	8192	12

Other modes could in principle be supported, such as 2 antennas, one polarization each, with 100 MHz bandwidth; however, these would require some hardware work and expense, and will be omitted unless there is a proven need for them.

Table 9.4 below gives the supported cross-correlation modes.

Table 9.4 Cross-correlator modes

Bandwidth (MHz)	Two polarizations, no cross-products		Two polarizations, all cross-products	
	Spectral channels	Resolution (kHz)	Spectral channels	Resolution (kHz)
800	1024	781	512	1563
100	8192	12	4096	24

Note that if 400 MHz and 50 MHz analog filters were provided, it would be possible to achieve a factor of two higher spectral resolution in any mode by operating the correlator in oversampled mode, which involves only throwing a hardware switch.

The minimum dump time supported by the correlator is 1.3 msec. However, the VME computer which receives the data from the LTA is thought to be capable of accepting the data at a rate which will give a minimum dump time of ~100 msec. The maximum integration time in the LTA before overflow is 85 seconds.

9.3 Interface Requirements

The correlator occupies one 24-inch EMI shielded rack. The four samplers are housed in a VLBA bin within the correlator rack, allowing stand-alone operation. Two extra VLBA bins, at present unwired, will be used to house the samplers at the antennas. Interfacing them to the correlator after the fiber optic link will be by means of special multi-signal cables.

The stand-alone correlator dissipates 1 kW and requires refrigerated air from the floor.

The correlator without samplers requires the following:

Clock input: 100 MHz sinewave, 50 ohms, 0 dBm (SMA connector)

Sync input: typically 1 PPS, TTL logic levels, into 50 ohms

Data input:

16 single-ended 2-bit 3-level ECL signals from each of 4 samplers (terminated with 50 ohms into -2V)

Communications: Ethernet interface

AC power: 30 amp 3-phase circuit for digital logic, 117 VAC for VME crate

The 4 samplers each require:

Clock input: 100 MHz sinewave, 2 V peak-to-peak, terminated in 50 ohms

RF input to samplers: 1.6 to 2.4 GHz, 50 ohms, -14 dBm

DC power:

0.03 A @ +5V
1.9 A @ -5.2 V
0.06 A @ +12 V
0.01 A @ -12 V
0.1 A @ +15V

Each sampler dissipates about 15W and requires modest forced-air cooling.