MMA RECEIVERS: SIS mixers

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Last revised 1999-April-15

Revision History:
1998-09-21: Added chapter number to section numbers. Placed specifications in table format. Added milestone summary.
1999-04-09: Revised date format to conform to MMA standard. Updated milestone table. Added description of new SIS junction fabricator.
1999-04-15: Updated milestone table. Added Figs. 5.3.4(c) and 5.3.4(d). Added subsections 5.3.2.3.1 and 5.3.2.3.2. Revised section 5.3.2.7.

Summary

This section describes the SIS mixers to be used in MMA receivers. They are expected to be used for all frequencies above 116 GHz. It is undecided whether SIS receivers will be used below this frequency (perhaps down to 68 GHz), or whether HFET amplifiers will be preferable for their greater immunity to interference and possible lower cryogenics cost. The goals for the design and development phase are to produce working prototypes of balanced, sideband-separating mixers with internal IF amplifiers meeting the general specifications.

Table 5.3.1 SIS mixer specifications

Item	Specification
Receiver noise temperature	Single sideband noise as low as possible (4 to 8 photons equivalent, depending on band)
Frequency bands covered	All atmospheric windows from ~68 to 1000 GHz; 230 GHz and 650 GHz bands during D&D phase
IF bandwidth	Goal: 16 GHz total per telescope, 8 GHz per polarization (8 GHz in a single sideband if possible; otherwise, 4 GHz per sideband)
Configuration	No mechanical tuners

Table 5.3.2 SIS mixer milestones for D&D Phase

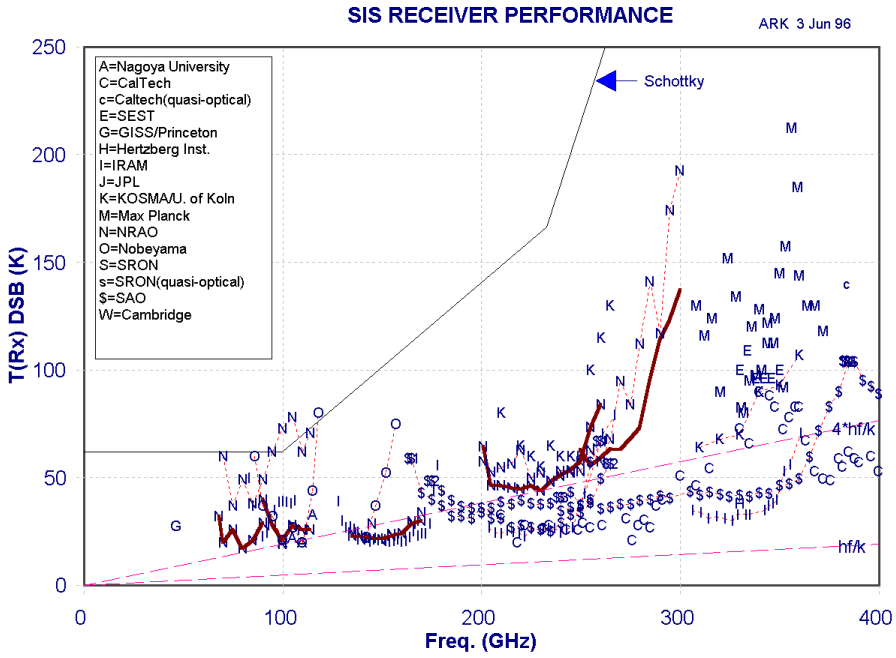
Deliver evaluation receiver 210-275 GHz mixer	1999-06-30
Deliver evaluation receiver 68-90 GHz mixer	1999-06-30
First MMIC integrated amplifier tests	1999-08-23
Preliminary Design Review	1999-09-07
Complete wafer evaluation circuits	1999-11-01
Complete automated mixer testing	1999-12-03
First 650 GHz building block mixer tests	1999-12-20
Complete integrated MMIC IF amplifier development	2000-01-31
Critical Design Review	2000-07-07
First 650 GHz SBS/balanced mixer tests*	2000-09-25
First 230 GHz SBS, balanced mixer tests*	2000-10-30
*SBS = sideband separating	

5.3.1 Performance

Figure 5.3.1 shows the DSB noise temperatures of SIS receivers reported in the last few years. The best fixed-tuned receivers have DSB noise temperatures in the range 2-4 hf/k up to ~700 GHz. Above ~700 GHz, receiver noise temperatures rise rapidly because of RF loss in the Nb conductors. Work on new materials is likely to improve high frequency results in the next few years (e.g., NbTiN for 700-1200 GHz).

Note that in calculating SBS *system* noise temperatures from DSB *receiver* noise temperatures, care must be taken to include the appropriate image input noise. The appropriate value of SBS receiver noise temperature is given by:

$$\mathbf{TR_{SBS} = 2TR_{DSB} + T_{image}}$$



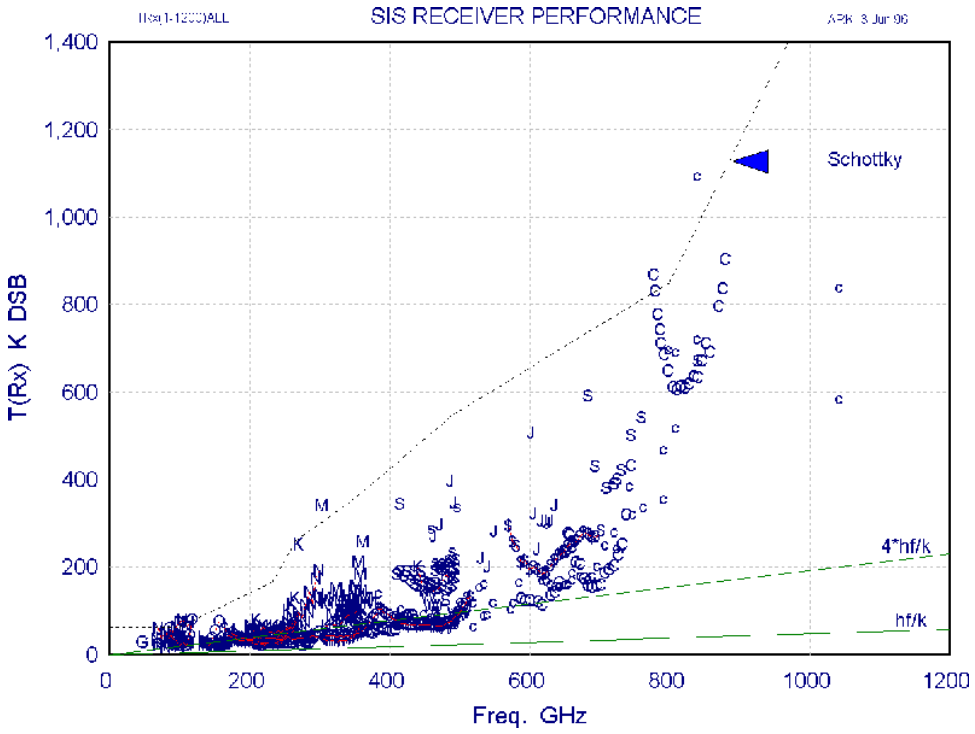


Figure 5.3.1 Reported SIS mixer receiver temperatures

Most of these receivers use a ~1.5 GHz IF, an exception being the SAO receivers which use 4-6 GHz. The IF for the MMA is tentatively chosen as 4-12 GHz to give the desired 8 GHz IF bandwidth. The final choice of IF will depend largely on the results of work now under way to develop an internal IF stage for SIS mixers which will allow isolators to be eliminated from the IF system. The best (individual) tunerless SIS receivers reported to date in the 150-400 GHz range have frequency ranges 1.37:1, 1.42:1, and 1.54:1. Their noise temperatures degrade quite precipitously beyond the band edges. In making the 80 receivers required for each band on the MMA, we cannot expect to achieve identical Tr vs. freq. characteristics, and the maximum bandwidth common to all 80 receivers will be somewhat less than that of the individual receivers. (Nb process control is something we are starting to work on with our SIS fabricators, but hitherto there has been little consideration given to such matters in SIS mixer production). It is hoped that by the time we start building the MMA receivers we will be able to achieve a 1.5:1 common bandwidth, but until this is actually demonstrated we should be conservative to ensure we do not end up with unexpected gaps in the frequency coverage.

5.3.2 Development

5.3.2.1 Capacitively loaded coplanar waveguide

To achieve wide RF bands (an upper to lower frequency ratio of 1.3 or greater) without mechanical tuning, a fully integrated (MMIC) mixer design is required. The resulting "drop in" mixer chips are relatively easy to mount in blocks in which they are coupled to RF and LO waveguides. Conventional microstrip MMIC technology is difficult to use above ~100 GHz because of the very thin substrates necessary to prevent coupling to unwanted substrate modes. The use of coplanar waveguide (CPW) circuits allows a thick substrate, but is prone to odd-mode resonances excited by bends or near-by obstacles, and has poor isolation between adjacent lines. CPW also requires inconveniently narrow gaps when a substrate of low dielectric constant (such as quartz) is used. To overcome these difficulties, we have developed capacitively loaded coplanar waveguide (CLCPW), a CPW with periodic capacitive bridges. The bridges are grounded at the ends, thus suppressing the odd CPW mode, but they also add a substantial capacitance per unit length to the CPW, which allows a desirable range of characteristic impedances to be obtained with convenient dimensions. Figure 5.3.2 shows a 200-300 GHz quadrature hybrid using CLCPW.

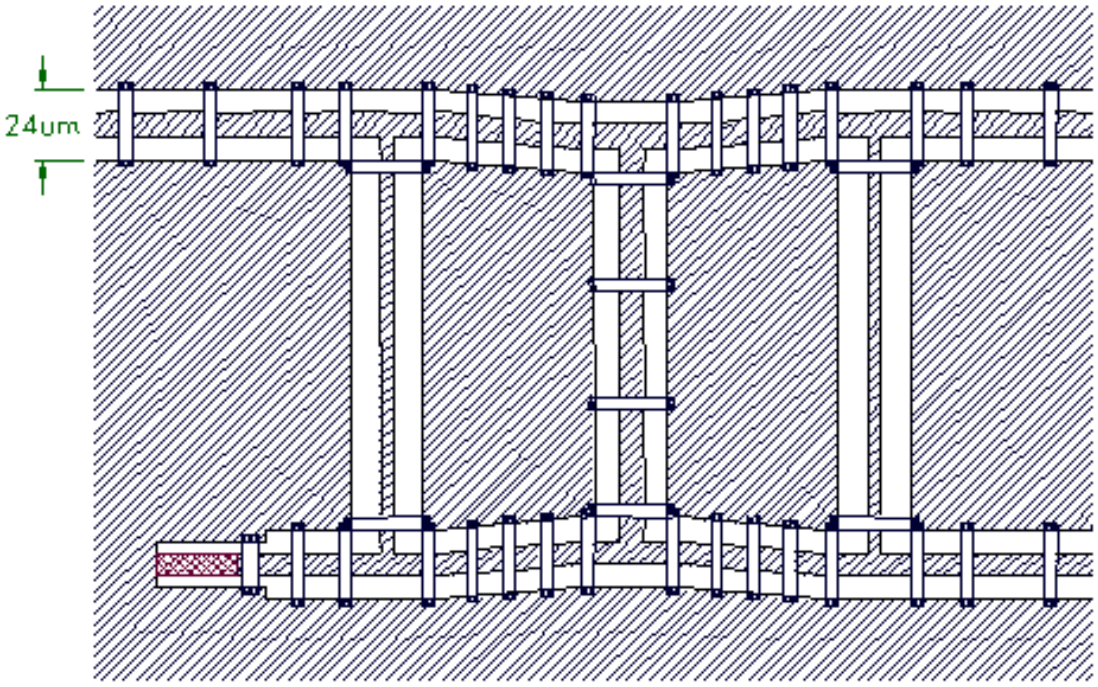


Figure 5.3.2. A 200-300 GHz quadrature hybrid using capacitively loaded coplanar waveguide (CLCPW). The bridges are 4 microns wide, and are connected to the ground plane at their ends. The fourth port (lower left) has a built-in matched termination. The substrate is 0.0035" fused quartz.

5.3.2.2 Sideband separating mixers

Even at the proposed site in Chile with its low atmospheric water vapor, atmospheric noise in the image band of an SIS receiver will add substantially to the system noise. The advantages of sideband separating mixers with their image terminated in a 4 K cold load have been discussed (see MMA Memos 168 and 170), and we expect to use sideband separating mixers in at least the lower frequency SIS receivers. A developmental MMIC 230 GHz sideband separating mixer is shown in Figure 5.3.3. The IF outputs from the mixer are combined in an external quadrature hybrid which phases the down-converted signals from the upper and lower sidebands so they appear separately at the output ports of the hybrid. A useful property of the sideband separating SIS mixer is that the sidebands can be swapped between the two outputs simply by reversing the polarity of the bias on one of the component mixers.

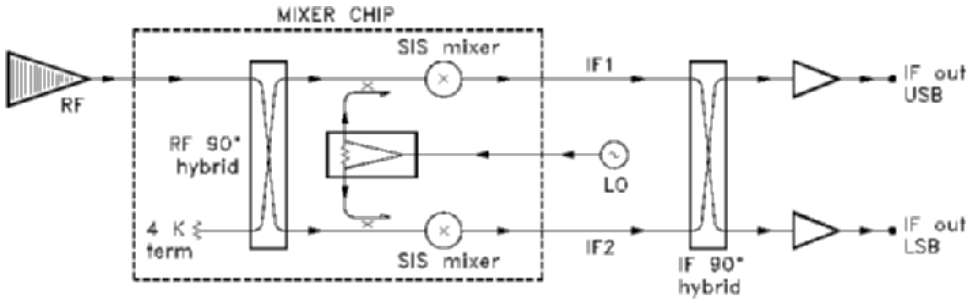


Figure 5.3.3(a). Block diagram of an SIS sideband separating mixer.

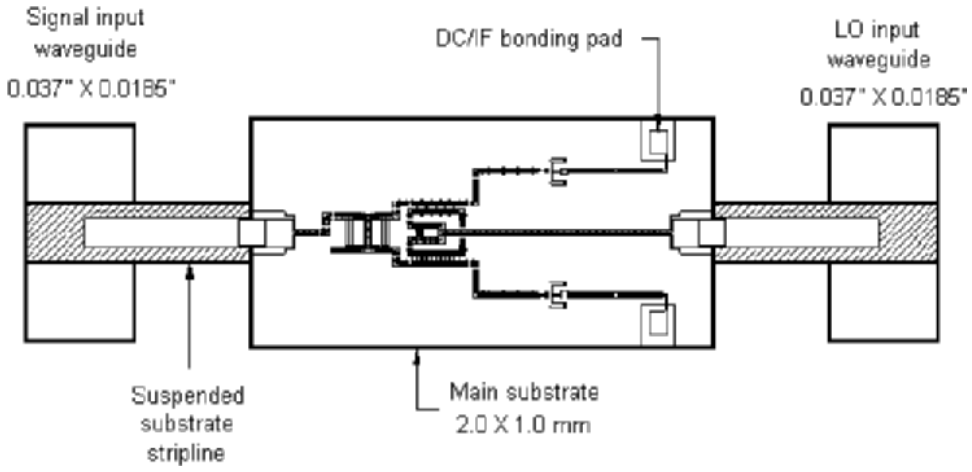


Figure 5.3.3(b). 230-GHz sideband separating mixer, showing the signal and LO waveguides, suspended stripline coupling probes, and the main substrate.

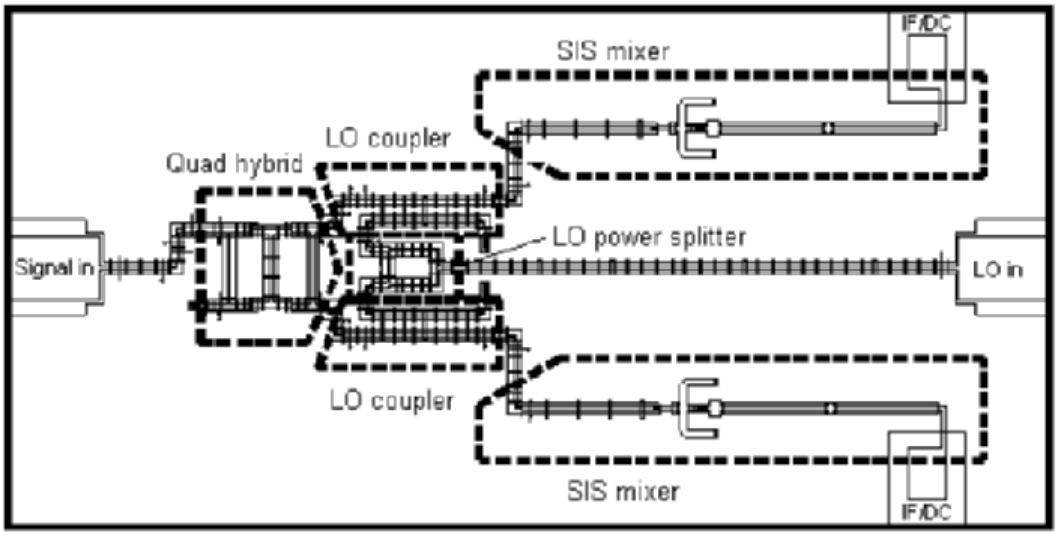
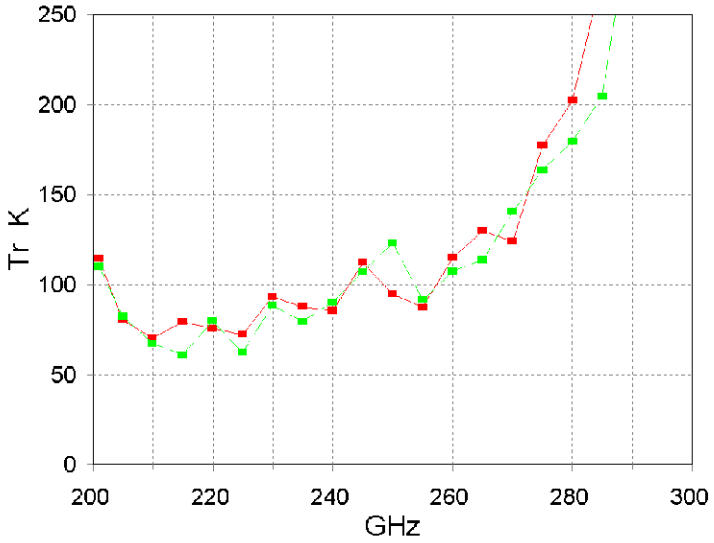


Figure 5.3.3(c). Substrate of the 230-GHz sideband separating mixer, showing the main components.



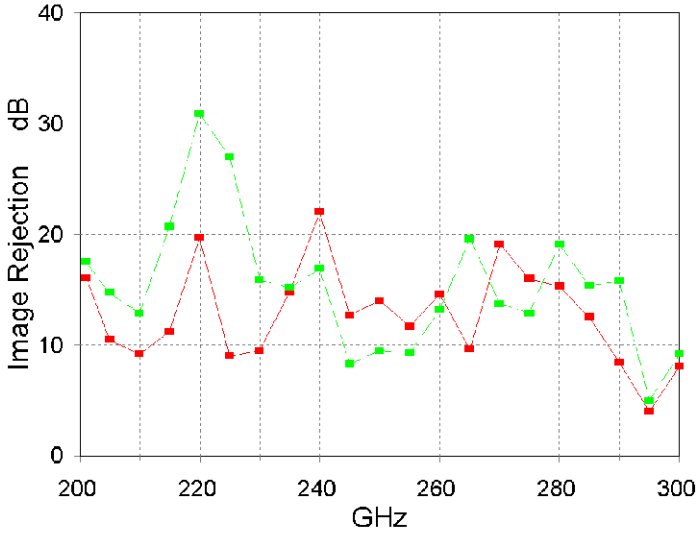


Figure 5.3.3(d) Receiver noise temperature and sideband separation for the experimental mixer.

5.3.2.3 Balanced mixers

The use of balanced SIS mixers has two potential advantages for the MMA. A balanced mixer requires ~17 dB less LO power than a single-ended mixer with a ~20 dB LO coupler, which greatly eases the task of developing wideband tunerless LOs. The other benefit of a balanced mixer is its inherent rejection of AM sideband noise accompanying the LO.

5.3.2.3.1 Single-chip (MMIC) balanced mixer

A MMIC balanced mixer design is shown in Figure 5.3.4.

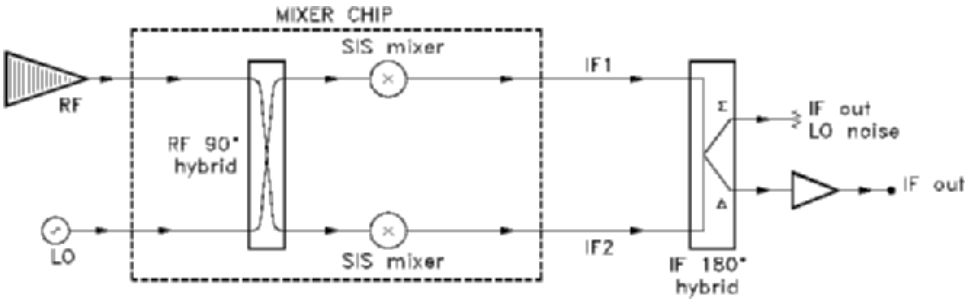


Figure 5.3.4(a). Block diagram of a balanced SIS mixer.

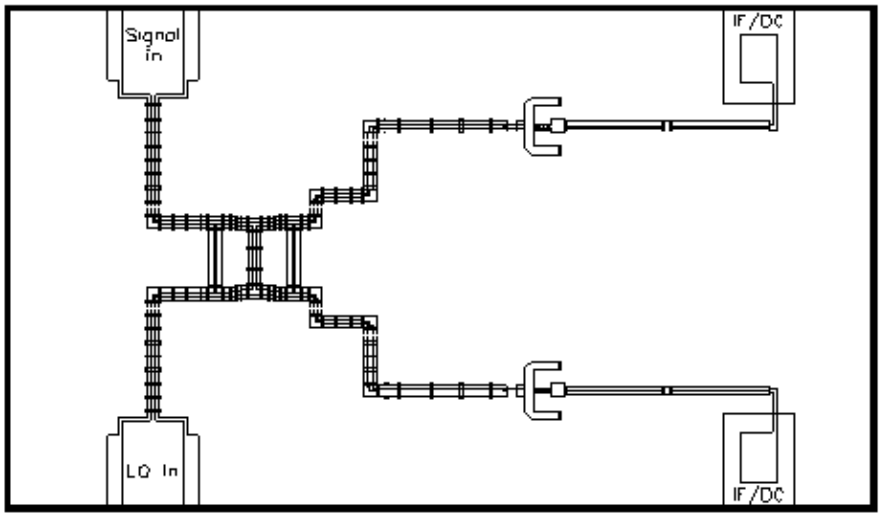


Figure 5.3.4(b). Substrate of a 230 GHz balanced mixer, showing the quadrature hybrid and two SIS mixers.

Results have been obtained on a prototype of the 200-300 GHz balanced mixer depicted above. The first such chip tested was tuned slightly high due to normal variation of wafer parameters, but it exhibits good LO noise rejection.

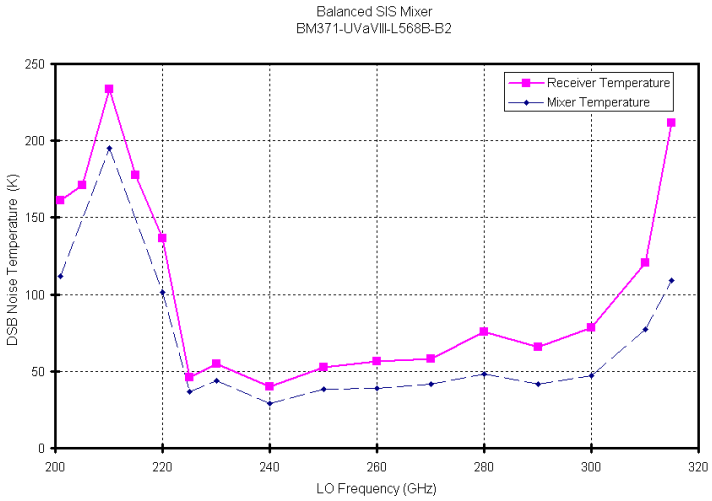


Figure 5.3.4(c). Receiver noise temperature.

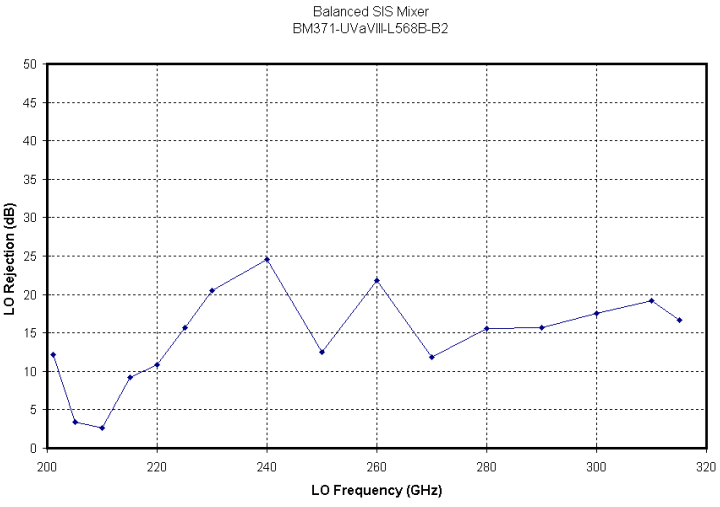


Figure 5.3.4(d). LO rejection of a balanced SIS mixer.

5.3.2.3.2 Balanced mixer using a waveguide quadrature hybrid

At frequencies above ~700 GHz, RF loss in Nb conductors will degrade the performance of MMIC balanced mixers (such as described above). We are developing a balanced mixer with a waveguide quadrature hybrid which is expected to have superior performance at high frequencies.

5.3.2.4 Sideband-separating, balanced mixers

Now that the designs of the sideband-separating and balanced mixers have been tested, we will design and build a mixer which incorporates both these features: a balanced, sideband-separating mixer. This will incorporate circuit elements whose designs have already been proven. It will provide for the MMA a mixer which requires a minimum of LO power, has good immunity to LO noise, and substantially reduces the contribution to the system noise of atmospheric noise in the unwanted sideband. A schematic diagram is shown in Figure 5.3.5. We expect that the mixer chip will be about 2 x 2 mm in size for 200-300 GHz.

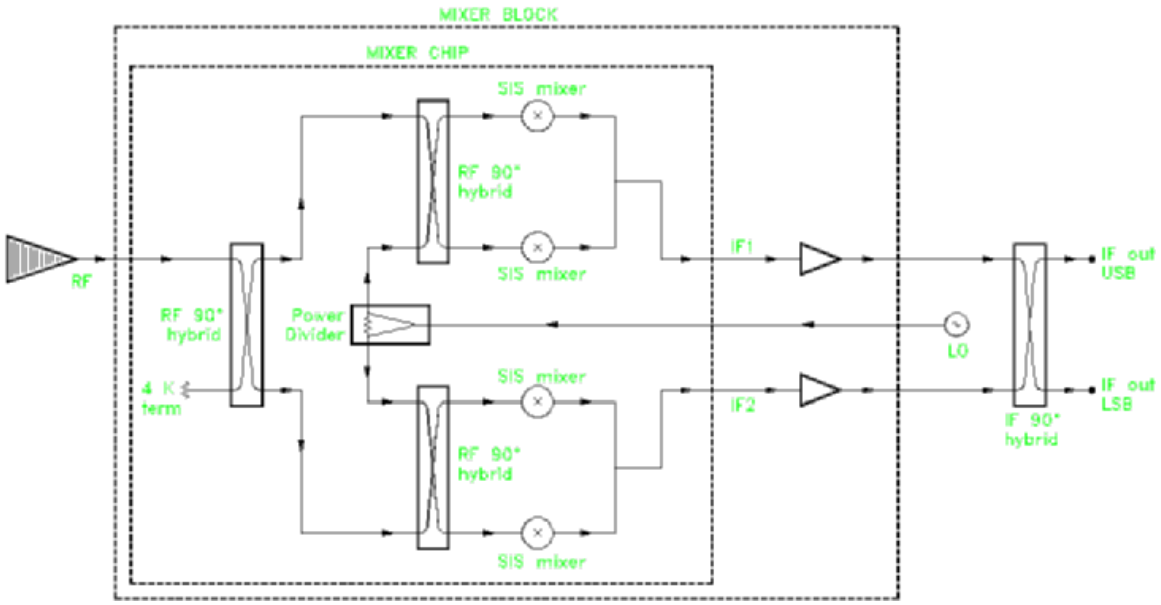


Figure 5.3.5. Block diagram of a balanced, sideband-separating SIS mixer.

5.3.2.5 Internal IF amplifier

Two options are being considered for the 8-GHz-wide IF in the SIS receivers for the MMA. The conventional approach uses an IF isolator between the mixer and IF amplifier, while a new scheme, developed at OVRO with assistance from the NRAO, uses an IF amplifier stage inside the SIS mixer block without an isolator. The latter scheme allows an IF covering more than an octave, tentatively 4-12 GHz. The need for an isolator in the conventional scheme forces the IF center frequency to at least 12 GHz (IF = 8-16 GHz) to achieve an 8 GHz bandwidth, probably with a significant noise penalty. The penalty is not simply a result of the increase in amplifier noise temperature at the higher frequency, but includes the noise from the cold termination of the isolator which is reflected from the mixer output.

The use of a high IF, as required by both the above schemes, imposes constraints on the output capacitance and inductance of the SIS mixer. In most SIS mixers, the RF tuning circuit and RF choke add substantial IF series inductance and capacitance in parallel with the SIS junction. We have developed an SIS mixer with low IF inductance and capacitance, and this design was used as a building block in the sideband separating and balanced mixers described above.

In collaboration with S. Weinreb at JPL, we have chosen an integrated IF amplifier design which, operating with our low-parasitic SIS mixer, should permit the MMA goal of 8 GHz instantaneous bandwidth per sideband to be realized. The MMIC amplifier chip employs a grounded gate first stage and is expected to give good performance over the 4-12 GHz target band. Tests are expected to being in late summer 1999.

5.3.2.6 Further plans

It is planned to continue the development of the 200-300 GHz sideband-separating, balanced SIS mixer with integrated IF amplifier until the goals of 5.3.1 are met. Once a number of these mixers have been evaluated, the frequency bands for the MMA will be frozen and new designs will be developed to cover those bands.

The choice of mixers for the test receivers to be used for antenna evaluation will depend on the progress by the time they are needed. Standard NRAO DSB mixers will be sufficient for antenna tests, and may be used. The IF for these test receivers will be 4-6 GHz -- consistent with existing IF component designs (bias-T's, isolators, amplifiers).

5.3.2.7 SIS mixer fabrication

University of Virginia: For many years A. Lichtenberger's group in the UVA Semiconductor Device Laboratory has been the primary fabricator of Nb SIS mixers designed at NRAO. They made the type 371 and 373 mixers for 200-260 GHz, now in use on the JCMT and NRAO 12 Meter telescopes, and most recently they made the single-chip balanced SIS mixers described in an earlier section. In addition to mixer fabrication, the UVA group are working with us on development of test circuits which will allow a rapid evaluation of the critical circuit parameters

on a wafer without the time-consuming testing of actual mixers; this will be particularly important in the production phase of the MMA. Also, UVA is exploring the feasibility of dicing quartz wafers by laser or RIE (reactive ion etching). Dicing in the conventional way -- using a dicing saw -- is extremely labor intensive and does not readily permit re-entrant shapes which would be advantageous for the MMA mixers.

SUNY Stony Brook: A second fabricator of Nb circuits for the MMA, J. Lukens' group at the State University of New York at Stony Brook, will provide new capabilities. The process used by the Stony Brook group differs substantially from those at UVA and JPL (who fabricated the sideband separating mixers described above). Stony Brook employs a "planarization" process developed at IBM which involves lapping the wafer after defining the junctions and depositing an SiO2 dielectric layer. The resulting surface is flat and the SiO2 thickness is accurate to within 0.015 micron. In addition, Stony Brook uses electron beam lithography for junction definition, which results in excellent uniformity of the smallest junctions required for submillimeter mixers. Over the years, there has been a great deal of attention paid to process control at Stony Brook, with the result that their SIS junctions are quite uniform across an entire wafer. The NRAO type 373 mixer design for 200-300 GHz (used in the sideband-separating and balanced mixer prototypes, as well as operationally on the 12 Meter telescope and JCMT) has been modified to suit the Stony Brook process and the first wafers are expected early in the summer of 1999.